Dual D-type flip-flop with set and reset; positive edge-trigger

74LV74

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) $<$ 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) $>$ 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LV74 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT74.

The 74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15pF V_{CC} = 3.3V	 11 14 14	ns
f_{max}	Maximum clock frequency	C_L = 15pF V_{CC} = 3.3V	76	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	24	pF

NOTES:
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV74 N	74LV74 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV74 D	74LV74 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV74 DB	74LV74 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV74 PW	74LV74PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset-direct input (active-LOW)
2, 12	1D, 2D	Data inputs
3, 11	1CP, 2CP	Clock input (LOW-to-HIGH), edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set-direct input (active-LOW)
5, 9	1Q, 2Q	True flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

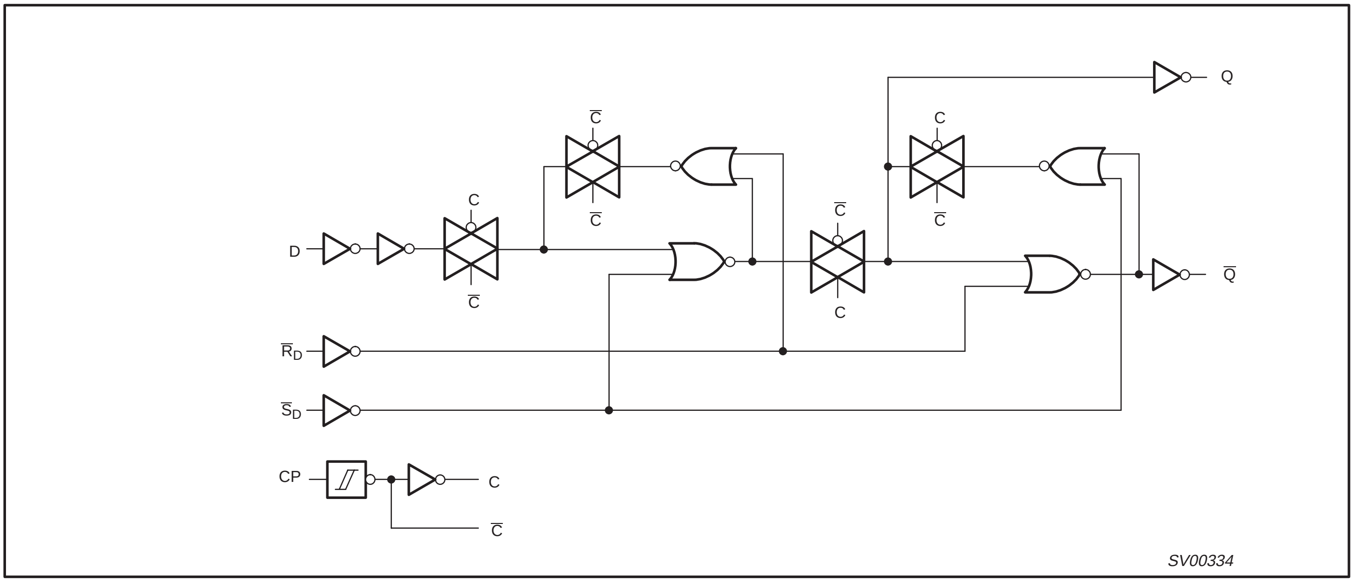
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

LOGIC DIAGRAM (ONE FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	V_I < –0.5 or V_I > V_{CC} + 0.5V	20	mA
$\pm I_{OK}$	DC output diode current	V_O < –0.5 or V_O > V_{CC} + 0.5V	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	–0.5V < V_O < V_{CC} + 0.5V	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; flip-flops	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		80	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

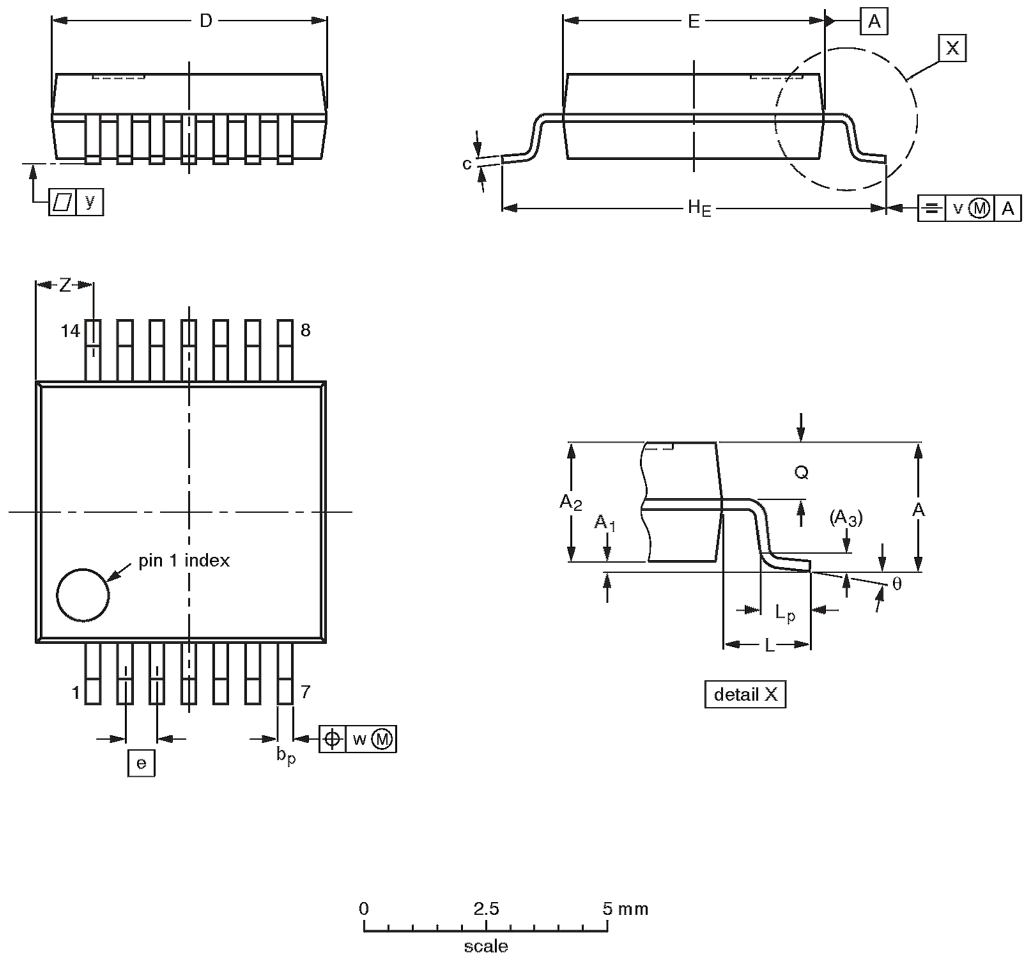
AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			$V_{CC}(V)$	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$	Figures, 1, 3	1.2	–	70	–	–	–	ns
			2.0	–	24	44	–	56	
			2.7	–	18	28	–	41	
			3.0 to 3.6	–	13[2]	26	–	33	
			4.5 to 5.5	–	9.5[3]	17	–	23	
t_{PHL}/t_{PLH}	Propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$	Figures 2, 3	1.2	–	90	–	–	–	ns
			2.0	–	31	46	–	58	
			2.7	–	23	34	–	43	
			3.0 to 3.6	–	17[2]	27	–	34	
			4.5 to 5.5	–	12[3]	19	–	24	
t_{PHL}/t_{PLH}	Propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$	Figures 2, 3	1.2	–	90	–	–	–	ns
			2.0	–	31	46	–	58	
			2.7	–	23	34	–	43	
			3.0 to 3.6	–	17[2]	27	–	34	
			4.5 to 5.5	–	12[3]	19	–	24	
t_W	Clock pulse width HIGH to LOW	Figure 1	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	6[3]	–	18	–	
t_W	Set or reset pulse width LOW	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	6[3]	–	18	–	
t_{rem}	Removal time set or reset	Figure 2	1.2	–	5	–	–	–	ns
			2.0	14	2	–	15	–	
			2.7	10	1	–	11	–	
			3.0 to 3.6	8	1[2]	–	9	–	
			4.5 to 5.5	6	1[3]	–	7	–	
t_{su}	Set-up time nD to nCP	Figure 1	1.2	–	10	–	–	–	ns
			2.0	22	4	–	26	–	
			2.7	12	3	–	15	–	
			3.0 to 3.6	8	2[2]	–	10	–	
			4.5 to 5.5	6	1[2]	–	8	–	
t_h	Hold time nD to nCP	Figure 1	1.2	–	–10	–	–	–	ns
			2.0	3	–2	–	3	–	
			2.7	3	–2	–	3	–	
			3.0 to 3.6	3	–2[2]	–	3	–	
			4.5 to 5.5	3	–2[3]	–	3	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	50	90	–	40	–	
			3.0 to 3.6	60	100[2]	–	48	–	
			4.5 to 5.5	70	110[3]	–	56	–	

NOTE:
1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.
2. Typical value measured at $V_{CC} = 3.3V$.
3. Typical value measured at $V_{CC} = 5.0V$.

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB